Наносистеми, наноматеріали, нанотехнології
Nanosistemi, Nanomateriali, Nanotehnologii
2026, т. 24, № 1, сс. 33–52
https://doi.org/10.15407/nnn.24.01.0033

PACS numbers: 03.67.-a, 07.50.Ek, 73.21.-b, 73.63.-b, 84.30.Bv, 85.35.Be, 85.40.Bh

A Study on 2-Dimensional 4-Dot 2-Electron QCA-Based Reversible-Circuit Design with Energy Dissipation Analysis

Md. Abdullah-Al-Shafi

University of Development Alternative (UODA),
80, Satmosjid Road,
Dhanmondi, Dhaka, Bangladesh

Since the scaling of archetypal transistors has extended its lowest point, the rational substitute for the complementary metal-oxide semiconductor (CMOS) technology to attain advance improvements in the circuits on the criterions of size, low power, and device density usage has turned into an imperative essential. In an extremely rapid expansion of VLSI technology, it is the requirement of the era to reach a consistent model with area and low-power consumption. Quantum-dot cellular automata (QCA) are a prospective nanotech archetype, which performs as a different resolution to regular CMOS that has several physical limitations and sets of circuits' bounds. QCA is an enticing nanotechnological paradigm because of its better switching frequency and faster-performing speed besides it comprise a novel approach for information transformation. This paper illustrates a new design of XNOR, TR, BVF gates, and 1-bit comparator by Feynman gate based on the QCA and CMOS technology, which is well organized compared with the earlier outline. To computer simulate and confirm the suggested gate, QCA designer and Microwind Lite engines are utilized. The quantum costs of the proposed typical circuits and their QCA designs are computed and compared that confirms that the proposed QCA designs have extremely low quantum cost compared to typical layouts. The power dissipation by the designs is estimated that confirms the prospect of QCA nanodevice performing as a substitute stage for the implementation of reversible circuits. The firmness of the proposed designs under thermal randomness is analysed, presenting the functioning efficacy of the designs. The designs have a propitious future in forming of nanoscopic-scale low-power consumption information transforming scheme and can be motivated advanced digital functions in QCA.

Оскільки масштабування архетипових транзисторів досягло свого найнижчого рівня, раціональна заміна технології виготовлення комплементарних інтеґральних схем типу метал–оксид–напівпровідник (КМОНп) для досягнення передових удосконалень у схемах за критеріями розмі-

ру, низького енергоспоживання та щільности використання пристроїв стала надзвичайно важливою. В умовах надзвичайно швидкого розвитку технології виготовлення надвеликих інтеґральних схем (НВІС) вимогою епохи є досягнення узгодженого моделю із площею та низьким енергоспоживанням. Клітинний автомат на квантових цятках (ККА) — це перспективний нанотехнологічний архетип, який має відмінну роздільчу здатність щодо звичайної КМОНп, але має й кілька фізичних обмежень і наборів меж контурів. ККА є привабливою нанотехнологічною парадигмою завдяки кращій частоті перемикання та швидшій роботі, а також представляє собою новий підхід щодо перетворення інформації. У цій статті проілюстровано нові конструкції логічних вентилів типу «виключне АБО–НЕ», «TR (Thapliyal–Ranganathan)», «BVF (межове векторне поле)» й 1-бітного компаратора за Фейнмановим вентилем на основі технології ККА та КМОНп, яка є добре організованою порівняно з попереднім планом. Для комп'ютерного моделювання та підтвердження запропонованого вентиля використовуються конструктор ККА та механізми Microwind Lite. Розраховано та порівняно квантові витрати стосовно запропонованих типових схем та їхніх конструкцій ККА, які підтверджують, що запропоновані конструкції ККА мають надзвичайно низькі квантові витрати порівняно з типовими схемами. Оцінено розсіяння потужности конструкціями, що підтверджує перспективність використання нанопристроїв ККА як заміни для реалізації оборотніх схем. Проаналізовано стійкість запропонованих конструкцій щодо теплової випадковости, що представляє ефективність функціонування конструкцій. Конструкції мають сприятливе майбутнє у формуванні схем перетворення інформації наноскопічного масштабу з низьким енергоспоживанням і можуть бути ініційовані розширеними цифровими функціями в ККА.

Key words: quantum-dot cellular automata, XNOR gate, TR gate, BVF gate, 1-bit Feynman gate comparator, power dissipation.

Ключові слова: клітинний автомат на квантових цятках, вентиль виключне АБО–НЕ, вентиль TR, вентиль BVF, 1-бітний компаратор за Фейнмановим вентилем, розсіяння потужности.

(Received 6 September, 2024)

1. INTRODUCTION

CMOS technology has been dominant the roost for several times and currently it is the reasonable technology in the microelectronic area. In current period, the goal is to scaling down to scheme a combined circuit, specifically rising the thickness of the circuit and thus it is essential to change from transistor to transistor less circuit. Nanotech has been the attentions of a widespread explore to replace the estimated restrictions of regular CMOS at the edge of the roadmap [1]. Moore's law expresses that the escalation of com-

bined circuits is at the level of $2X$ per each 18 months, where X denotes the number of transistors per entity area [2]. As the manifested restrictions of this technology, *i.e.*, fault analysis complications, speed, oxide thickness, and extent overhead; enlarged with the better circuit intricacy as shift to an advanced stage of system unification, the effective substitute for the CMOS has grown into an instant requirement. Quantum-dot cellular automata [3, 4] that has currently been identified as one of the elites arising technologies with conceivable applications in imminent computing [5, 6] for its specific speed, smaller space, and very low power utilization in different computational functions [3]. Quantum dots are small elements generally (2–10 nm) composed from semiconductor resources, which show microelectronic properties. Their lesser size denotes that electrons do not have to move as far as equated with higher particles; so, electronic tools conceived by quantum dots can perform swifter. Logic circuits created from quantum dots is one of the utmost contemporary technologies that is being scrutinized and circuits occupied in quantum-based computers can be obtained from the quantum dot circuits. This technology is an assuring computing concept which has huge applications in evolving technologies, *e.g.*, quantum computing, optical information handling, digital signal processing, optical computing, DNA computing, *etc.* [7–9].

In information-lossless circuit, the input vector is produced from each output vector, and vice versa. It has presented [10] that the cost of each bit of information depletes the energy of $kT\ln 2$ [J], where k is Boltzmann's constant and T is the pure temperature. At room temperature, the extent of heat produced because of a single bit of information loss is minor, that is estimated as $2.9 \cdot 10^{-21}$ J, but it is not insignificant. Later, it is indicated [11] that the energy falls could be avoidable, if the computation is carried out with no cost of information. Molecular QCA can function at room temperature [12] and an amount of QCA based circuits have been suggested based on QCA wires, inverter and majority gate. Several QCA occupying combinational [13–18] and sequential [19–22] designs have been projected in recent times, though, reversible circuit form [23–28] in QCA are still uncharted research field. In this paper, three inventive QCA circuit models and comparator have been proposed that is more effectual in terms of total cell numbers, space and complexity corresponding to the earlier design [40–42] and their performance has been tested using the QCADesigner and Microwind. Besides, analyses of the proposed reversible circuits and their corresponding QCA designs are presented based on quantum cost and the heat-energy dissipation as well as the output polarization and consistency of the designs is measured under thermal randomness.

This article is organized in six sections. Section 1 presents the introduction of QCA. Section 2 discusses a concise synopsis of the

QCA structures. In section 3, the approach and urged layout of the proposed design in QCA are discussed. The simulation outcomes as regards different characteristics of these shown designs are described in section 4. Section 5 describes the quantum cost and power dissipation of proposed QCA layout. Lastly, section 6 concludes this analysis with imminent work.

2. QUANTUM-DOT CELLULAR AUTOMATA

All QCA provisions logic cases not as voltage phases but rather based on the point of separate electrons. The central QCA features are QCA wire, inverter and majority gates. Cells are the elementary entities of QCA based circuit and they are usually constituted of four quantum dots positioned at the corners of a square pattern. Each cell is charged with two supplementary electrons, which channel from one low-potential state to another across a high-potential direction and a back plane voltage switches the cell occupancy.

The electrons will be located in transversely to each other owing to reciprocal repulsive electrostatic power, possessing the utmost distance between them. A remote cell may be in one of two corresponding energy positions. These positions are called cell polarizations $P = +1.00$ and $P = -1.00$ as shown in Fig. 1, *a*. $P = 0$ denotes an unpolarised cell, which covers no information. A cell polarization P is -1, if the electrons are involved the locus 2 and 4; in the same way, a cell polarization P is $+1$, if electrons are involved the position 1 and 3. The cell-polarization equation [29] is presented below:

$$P = \frac{(\rho_2 + \rho_4) - (\rho_1 + \rho_3)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)}, \quad (1)$$

where the charge at dot i denoted by ρ_i. QCA wire encompasses of series of cells, where the cells are united one after another [26, 27]. QCA wire is employed to transfer signal from one position to another in a circuit. Logical charges are moved from cell to cell because of the Coulomb contacts. There are two modes of alignments in a QCA wire namely binary wire and inverter chain. QCA wires can be either originated up of 45° cells or 90° cells as shown in Fig. 1, *b*. In case of inverter, if two cells point at 45° with regard to each other, their contact will be reverse and, for that, these cells are mostly employed for coplanar wire crossings.

The inverter is a pattern of cells that reverse the input topology from one logic to another. Usually, two categories of inverter are applied [28] that has been operated for the realization of several structures as an essential cell [14], [16], [28], [31]. The inverter can be designed by fixing QCA cells at 45° position [31] as appeared in

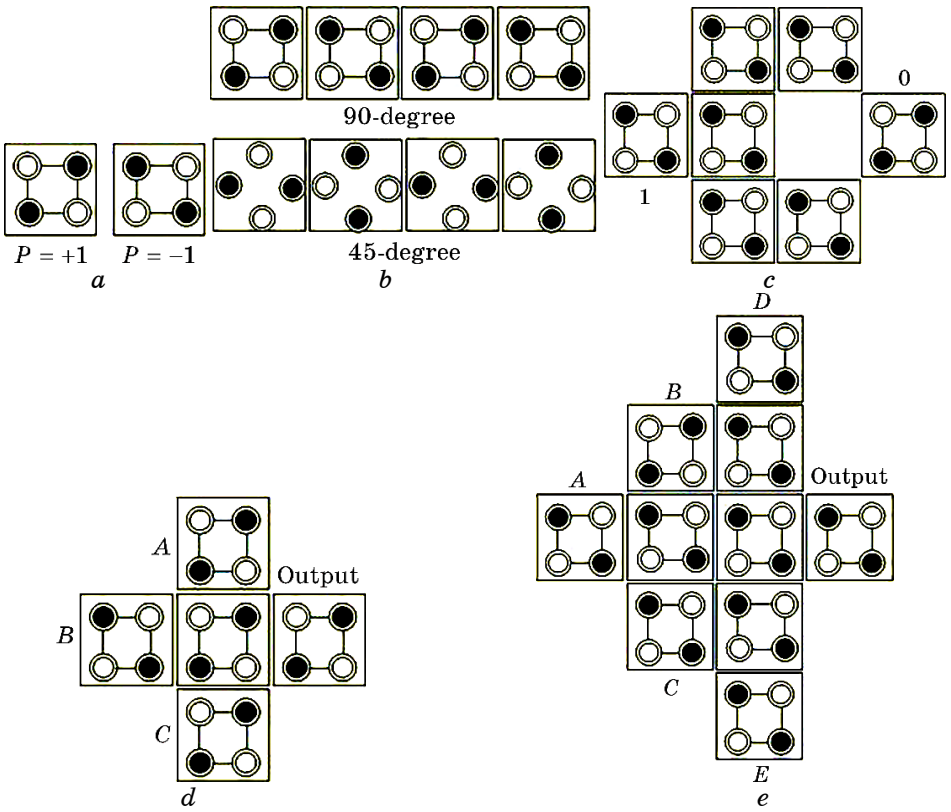

Fig. 1. QCA logical designs: *a*—plain cell; *b*—wires; *c*—potent inverter; *d*—3-input majority gate; *e*—5-input majority gate.

Fig. 1, *c*, which is potent and mostly used in circuit design. The logic values 0 and 1 transformed to 1 and 0 because of electrostatic repulsion. Binary wire transfers signal with similar polarity from one place to another, while inverter chain reverses the input cell polarity when odd figures of cells are employed in it. Majority gate is assembled of five QCA cells; a central cell, one output, and three inputs. Polarity of the middle cell, as identified as device cell, is imposed by the Coulomb repulsion to be equivalent to the output cell. The device cell at the centre of the gate has its least energy, when it accepts the polarization of the majority of the three input cells, since this is the formation, where the repulsion between the electrons in the three inputs cells and the electrons in the device cell is lowest.

Table 1 presents the output and input cells arrangements; '1' signifies logic '1' and '0' implies logic '0' in Table 1. So, an arrangement of inverter and majority voter is appropriate to con-

TABLE 1. Truth table of three input majority gate.

A	*B*	*C*	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

struct an extensive logic set for scheming of any circuit.

Majority voter can operate as AND or OR logic gate depending on the static polarity of the third input of the majority voter as presented in Fig. 1, *d*. The logical equation of the 3-input majority gate can be stated as follows:

$$MV(A, B, C) = AB + BC + AC. \quad (2)$$

Logical 2-input AND and 2-input OR functions can be executed using majority voter by putting one input cell to binary '0' and '1', subsequently. Equations (3) and (4) express the 'AND' and 'OR' gate process, while $C = 0$ and $C = 1$:

$$MV(A, B, 1) = A + B, \quad (3)$$

$$MV(A, B, 0) = AB. \quad (4)$$

The satisfying attainment of realizing a 3-input majority voter with five QCA cells inspired the analysts to hypothesize an inventive configuration for 5-input majority voter. Later, a specific layer [30] 5-input majority voter utilizing ten cells executed in a precise cell layout, which is displays in Fig. 1, *e*. The logic equation of the 5-input majority voter can be expressed as follows:

$$MV(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + \\ + ADE + BCD + BCE + BDE + CDE. \quad (5)$$

To form more complicated QCA devices, the location of QCA cell is not only essential also needs to coordinate the information, so that evade having a signal extending a logic gate and proliferating before the other inputs move the gate. This specific characteristic is particularly imperative in QCA circuits, ensuring its accurate function, and this aspect is attained by QCA clock. The clock is an elec-

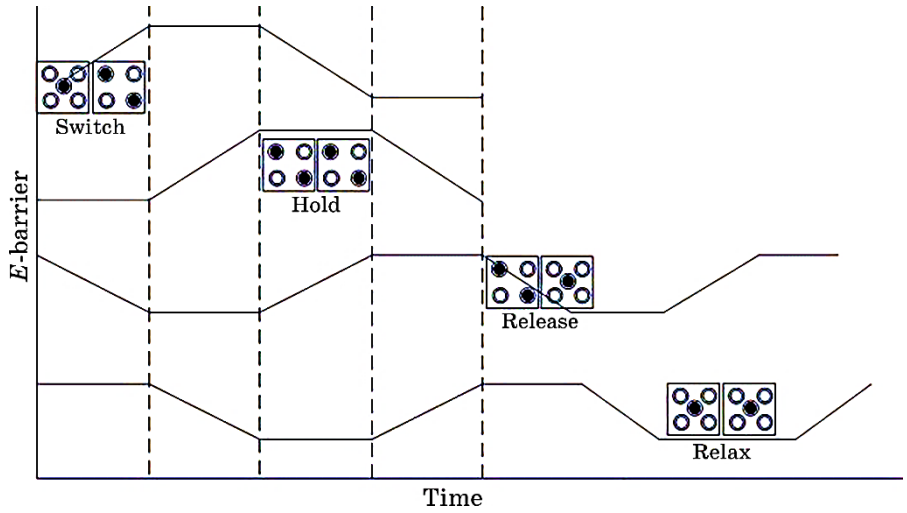

Fig. 2. QCA switching between four stage clocking.

trical region that switches the channelling barriers within the cell, therefore, retaining control, when a cell may or may not be polarized. QCA clocking is produced of four periods lagging by $\pi/2$ [32, 33] (see Fig. 2) that generates an innovative way to conceive nanocircuits distinct from the regular CMOS circuits [34]. In each region, a certain potential can adjust the barriers between the dots, and the organization of clock zones allows a group of QCA cells to construct a particular calculation; then, its positions are stationary and its outputs can be applied as inputs to the following clock zone.

Switch period: the barrier between dots of QCA cell is elevated and the dots are motivated by the electron of its adjoining as well as electron begins channelling between dots; thus, the cell turns into polarized. *Hold period*: cell barrier stays high and electron cannot channel between dots, and the cell keeps its existing position. *Release period*: barrier between dots is decreased, the electron can channel within dots and cell comes to be unpolarised. *Relax period*: barrier remains at lowered and cell stays in unpolarised position.

3. METHODOLOGY AND PROPOSED DESIGN

An assay is fulfilled to acquire the required devices and selected to realize the suggested design. The composition level is permitted applying a number of approximate simulators as the nonlinear approximation methods and bistable simulation device. However, these approximate do not develop the specified measures because these methods are iterative. In time, the QCA designer is preferred and

this simulation tool is demonstrated [35]. The bistable simulation tool has been occupied in the simulation interface between cells; clearly, the contact force linking two cells decomposes contrariwise with the fifth power of the length untangling them. During this estimation, not all the cells impact is counted and cells within the radius of R are being measured. For i-th cell, the scientific pattern is depicted by the following Hamiltonian:

$$H_i = \sum_j \begin{pmatrix} -\frac{1}{2} P_j E_{i,j}^k & -\gamma \\ -\gamma & \frac{1}{2} P_j E_{i,j}^k \end{pmatrix}, \tag{6}$$

where P_j is the polarization for cell j, $E_{i,j}^k$ is the kink energy between the cells (i and j), and γ is the channelling energy. For every cell i, the amount of the Hamiltonian is over all cells (*viz.*, j) in its radius of effect, R. The Jacobi algorithm has been utilized to obtain the eigenvectors and eigenvalues of the Hamiltonian. At the layout level, small QCA block is designed and simulated for analysis of its precision. Later, these QCA blocks are unified together through QCA wire to manage the proposed composition. Finally, the consistency of the design is surveyed by the QCA designer. The simulation outcome the essential waveform for the logical circuit and during simulation, it created few criterions that contains default standards as the cell size, layer separation, relative permittivity, samples number, *etc*. The proposed design in CMOS is formulated and simulated using Microwind [36] tool. This engine is standard and appropriate to achieve the surface of the diverse logic circuit. In this paper, the waveform of the proposed layout seamlessly fits the logical input and output.

A gate is identified information-lossless or reversible, if there is a one-to-one correspondence between its number of output and input assignments. Information-lossless circuit stimulates a certain set of input vector for each set of the output vector and it accomplished common attention since their possibility to subside the dissipation of power. In this paper, a significant layout of BVF and XNOR circuits is organized. The XNOR gate (also denoted as ENOR or Exclusive NOR) is a digital logic gate with two or more inputs and one output, which presents logical equivalence. The result of an XNOR gate is valid, when all of its inputs are false or all inputs are true. If certain of its inputs are true and others are false, then, the outcome of the gate is false. Two input XNOR gate can be achieved by an inverter and three majority gates as presented in Fig. 3.

Among these majority voters, two majority gates are effected to perform like OR gates by making one input equivalent to '1' and

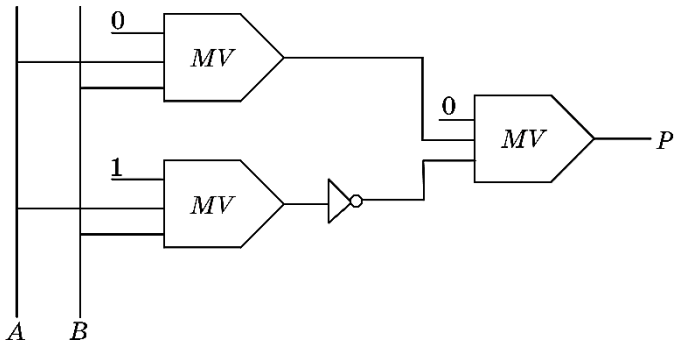

Fig. 3. Proposed layout of XNOR gate in QCA.

the last majority gate is effected to perform like an AND gate by composing the third input equivalent to '0'. The logical equation of XNOR gate is as follows:

$$P = (AB) + (A + B)' = AB + A'B'. \tag{7}$$

The TR gate (also familiar as Thapliyal and Ranganathan gate) [37] is a 3-input and 3-output reversible gate shown in Fig. 4. The

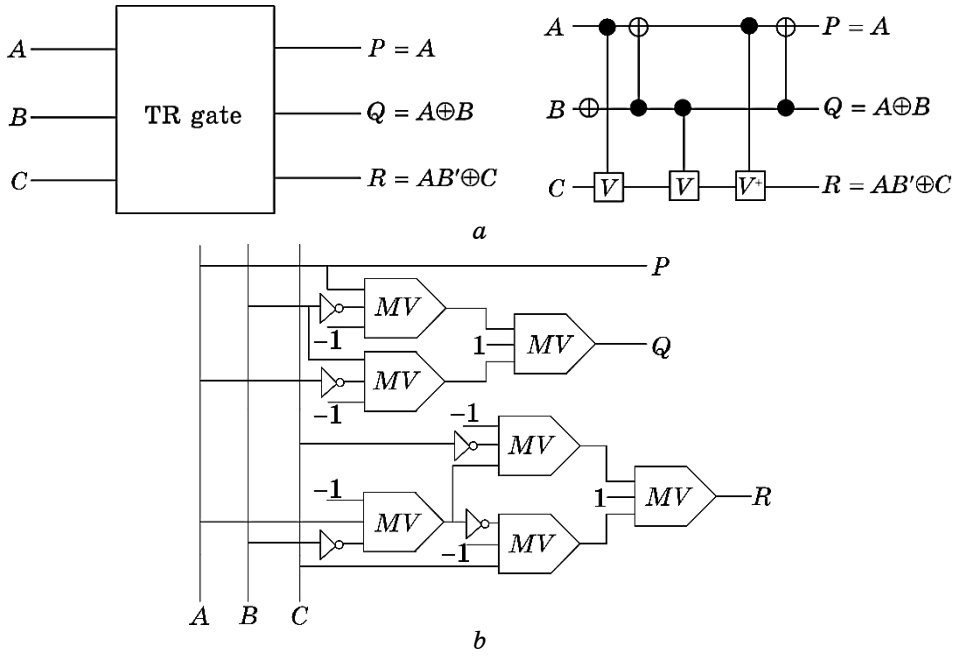

Fig. 4. Block diagram of (*a*) TR gate; (*b*) proposed layout of TR gate in QCA.

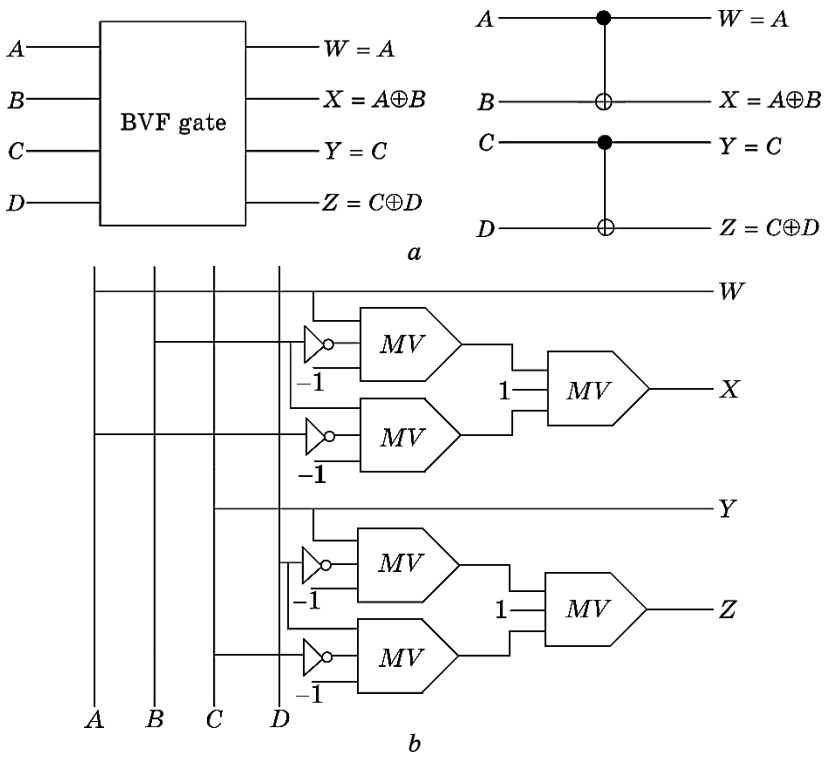

Fig. 5. Block diagram of (*a*) BVF gate; (*b*) proposed layout of BVF gate in QCA.

input vector of TR gate is stated as $I_v(A, B, C)$ and the corresponding output vector is $O_v(P, Q, R)$. The outcome is denoted as $P = A$, $Q = A \oplus B$ and $R = AB' \oplus C$. The quantum cost of TR gate can be realized from the quantum execution of Toffoli gate [38]. Using 2 NOT gates and 1 CNOT and Toffoli gate, the cost of TR gate is achieved. Therefore, the cost will be quantum cost of 1 Toffoli gate + quantum cost of 1 CNOT gate, *i.e.*, = 6.

BVF gate also identified as 4×4 double XOR reversible logic gate [39]. The input vector is defined as $I_v(A, B, C, D)$ and the output vector is $O_v(W, X, Y, Z)$. The result is expressed as $W = A$, $X = A \oplus B$, $Y = C$ and $Z = C \oplus D$ as shown in Fig. 5. This gate can be operated for the replication of the expected inputs to meet the fan out conditions, and the gate is employed to model the operand bits and the number of gates needed to copy is decreased by 50% with similar quantum effort.

A 1-bit comparator takes two 1-bit numbers, for example, A and B as inputs and generates an output specifying whether $Y_1 = AB'$, $Y_2 = A$ NOR B, and $Y_3 = A'B$ for $A > B$, $A = B$, and $A < B$, correspondingly. Figure 6 illustrates the simulated layout of proposed XNOR,

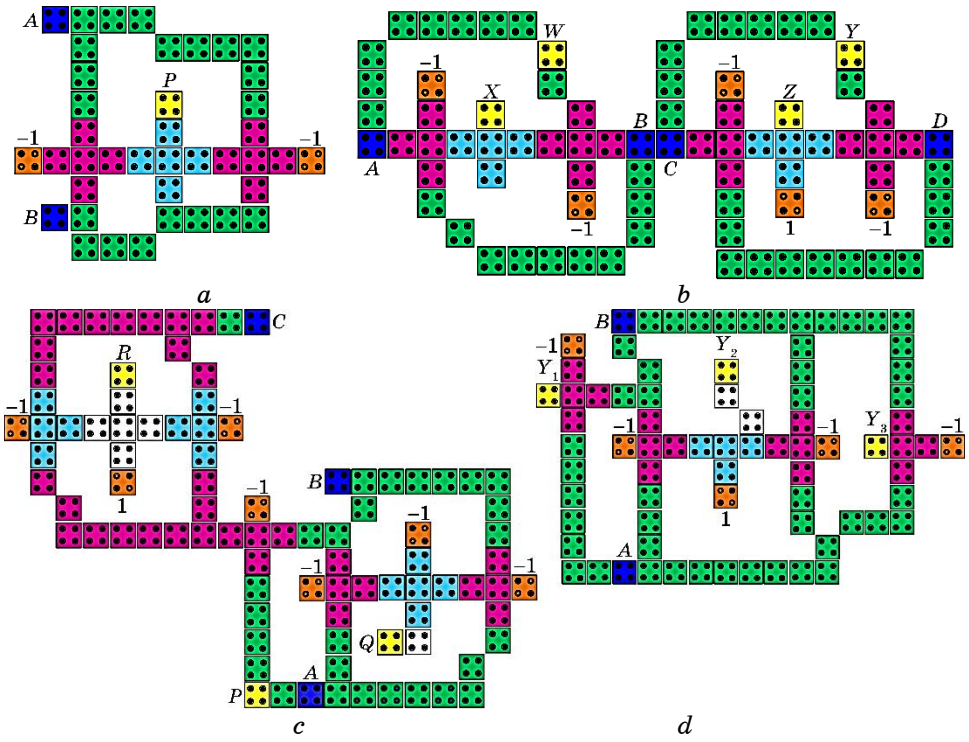

Fig. 6. QCA simulated circuit design of proposed: (*a*) XNOR gate; (*b*) BVF gate; (*c*) TR gate; (*d*) 1-bit comparator by Feynman gate.

BVF, TR, and 1-bit comparator in Feynman gate, respectively, where: in Fig. 6, *a*, *A*, *B* and *P* are the input and output cell, correspondingly; in Fig. 6, *b*, the inputs are *A*, *B*, *C*, *D* and their equivalent outputs are *W*, *X*, *Y*, and *Z*; in Fig. 6, *c*, the inputs are *A*, *B*, *C* and their corresponding outcomes are *P*, *Q*, *R*; in Fig. 6, *d*, inputs are *A*, *B* and their corresponding outputs are Y_1, Y_2, and Y_3. In circuit composition, two static polarizations $P = +1$ and $P = -1$ are operated that are occupied to shift the logic form.

4. SIMULATION-RESULTS' ANALYSIS

The design has been functionally fabricated and simulated using the QCA designer that presents some criterions in the coherence vector and bistable approximation, which are the default features in QCA designer. These parameters are exhibited in Table 2. The decisive QCA functioning design of the proposed XNOR, BVF, TR and 1-bit comparator design of Feynman gate is illustrated in Fig. 7, *a*, *b*, *c* and *d*, respectively. The first layout involves of 40 cells and cover-

TABLE 2. Parameters of bistable approximation and coherence vector.

Criterion	Value
Size of cell	20 nm
Dot diameter	5.000
Number of samples	12800
Temperature	1.00 K
Relaxation time	$1.000000e^{-15}$ s
Convergence tolerance	0.001000
Radius of effect (bistable)	65.000000 nm
Time step	$1.000000e^{-16}$ s
Relative permittivity	12.900000
Layer separation	11.500000
Radius of effect (coherence)	80.000000 nm
Clock amplitude factor	2.000000
Clock high	9.800000*e*–022
Clock low	3.800000*e*–023
Lower threshold [0]	–0.500
Upper threshold [1]	0.500
Maximum iterations per sample	100
Total simulation time	$7.000000e^{-11}$ s

ing an extent of 0.04 μm^2, the second layout involves of 79 cells and covering an extent of 0.07 μm^2, the third layout involves of 92 cells and covering an extent of 0.12 μm^2 and the comparator involves of 78 cells and covering an extent of 0.08 μm^2. It is very essential to create an operationally firm layout in QCA functions. There are certain concerns realized into account to raise the design stability. When building models in QCA, a substantial attempt should be made to maintain the wire length in a specified clocking region to a minimum. For smaller wires, it is almost certainly that all cells creating up the wire will switch effectively.

The scheme of proposed design in CMOS is organized in Fig. 8, *a*, *b* and *c*, respectively, which is performed using Microwind Lite engine, a fast-systematized EDA tool for front and back-end chip fashion into an integrated flow. Table 3 explains the complication of the proposed design respecting the number of cells, majority voters, clocking zones and covered area applied to perform the layout.

Table 4 illustrates that the proposed XNOR has improvements of 38.46% and 42.85% in terms of total cell and area respectively, relative to the design proposed in Ref. [40]. Similarly, the improvements of BVF, TR and 1-bit Feynman gate comparator are 3.66% and 30.00%, 18.58% and 40.00%, 10.36% and 3.00%, correspondingly, proposed in Refs. [41, 42].

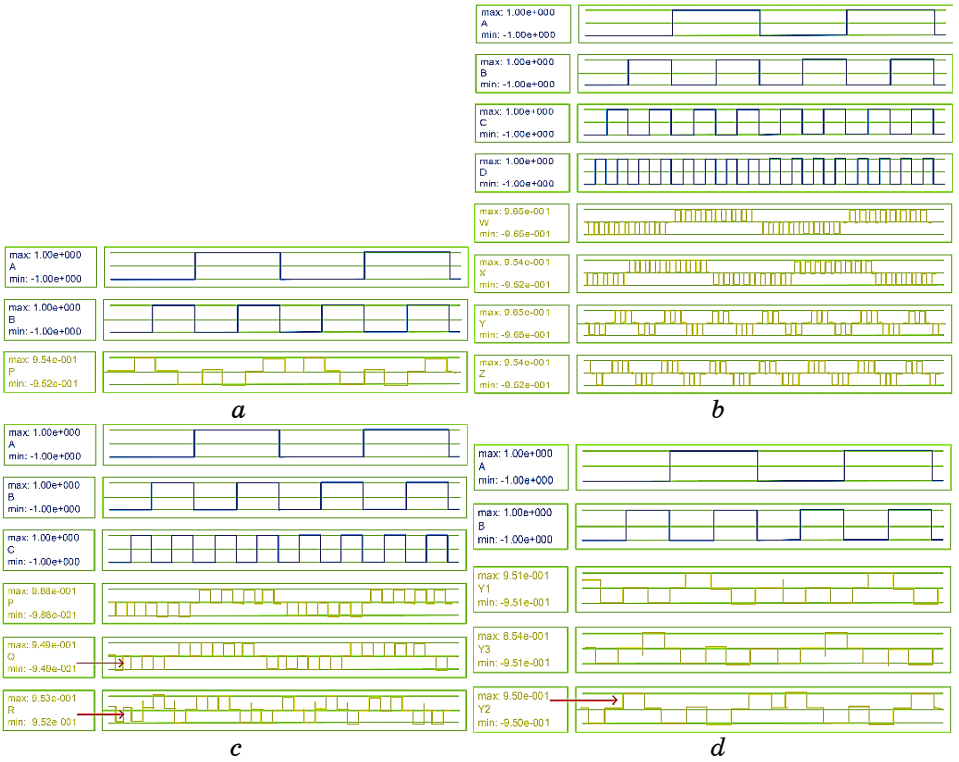

Fig. 7. QCA outcome of the proposed: (*a*) XNOR, (*b*) BVF, (*c*) TR, and (*d*) 1-bit comparator design of Feynman gate.

5. DESIGN QUANTUM COST AND POWER DISSIPATION OF THE PROPOSED CIRCUIT AND ITS QCA OUTLINE

The quantum cost of 2×2 reversible circuit is counted one, however all reversible 1×1 circuit have a quantum cost of zero [24]. Thus, the quantum cost of XNOR gate is one. BVF and TR gate have a quantum cost of two and four respectively.

The proposed 1-bit comparator in Feynman gate is organized of one Feynman gate and three reversible NOT gate, Thus, the proposed 1-bit Feynman gate comparator has a quantum cost of (1×1 + 0), *i.e.*, 1.0. The corresponding quantum costs of the proposed layouts are figured in Table 5.

The proposed XNOR design has area of 0.04 μm^2 and latency of 0.75. Therefore, the cost of the proposed QCA design is area×latency 2 = 0.04×0.752, *i.e.*, 0.022. The proposed QCA BVF circuit has an extent of 0.07 μm^2 and latency of 0.50, which reason the quantum cost of the proposed circuit is = 0.07×0.502, *i.e.*, 0.017.

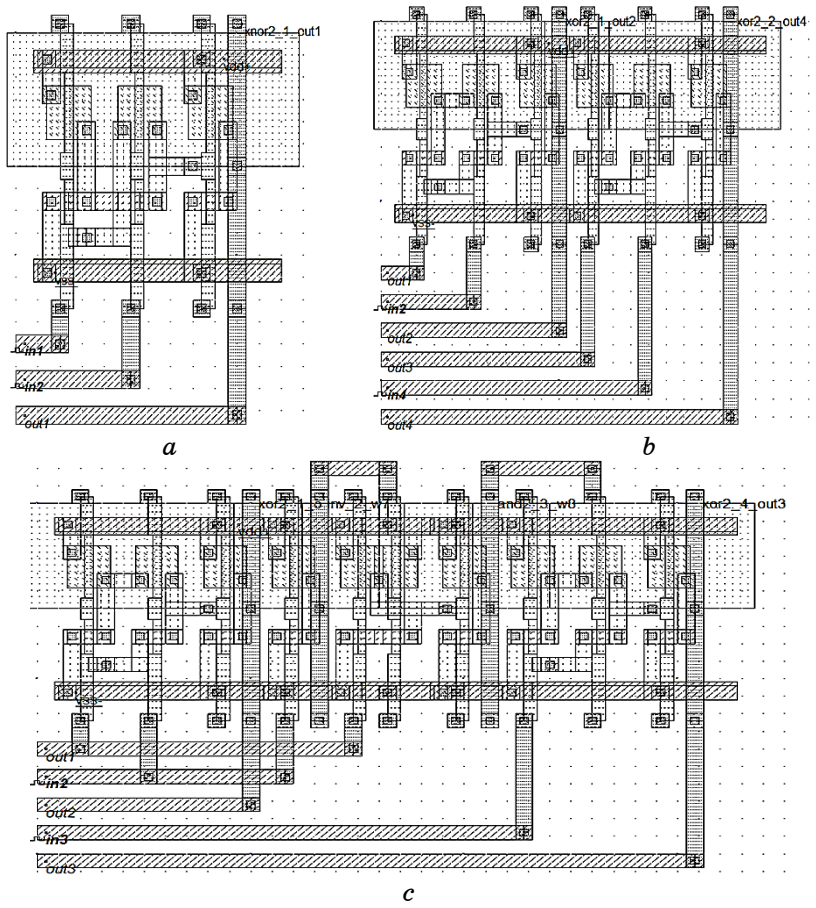

Fig. 8. Simulated circuit design in CMOS: (*a*) XNOR gate; (*b*) BVF gate; (*c*) TR gate.

Just as, the costs of other circuits are estimated, and the results are presented in Table 5. The quantum cost of XNOR gate in typical design is 1.0, however in QCA-based design, it is of 0.022. For 1-bit Feynman gate comparator, typical layout has a quantum cost of 2.0, but QCA-based layout requires a quantum cost of 0.020. Table 5 illustrates that the quantum cost of QCA-based layouts is lower than that of traditional layouts. Hence, QCA-based designs are cost effectual with corresponding to quantum cost. The relevant comparison is also illustrated in Fig. 9.

The dissipation of power by each QCA cell in a circuit is identical [43]. Therefore, in a range of connected QCA cells, the total dispelled power can be projected by adding the dispelled power of each cell within the range. The circuit power consumption is reliant on

TABLE 3. Performance criterions of proposed design.

Parameter	Cell intricacy	Clock used	Time delay	Covered area, μm^2	Area in CMOS, μm^2	Improvement (in times)
Proposed XNOR gate	40	3	0.75	0.04	21.9	548
XNOR gate [41]	65	4	1	0.07		
Proposed BVF gate	79	3	0.50	0.07	47.6	595
BVF gate [41]	82	3	0.50	0.10		
Proposed TR gate	92	4	1	0.12	71	592
TR gate [42]	113	4	1	0.20		
Proposed 1-bit Feynman gate comparator	78	3	0.50	0.08	—	
1-bit Feynman gate comparator [42]	87	4	0.50	0.11		

TABLE 4. Complexity of the proposed designs.

Proposed design	Cell area, μm^2	Area use, %	Cell improvement, %	Area improvement, %
XNOR gate	0.013	32.50	38.46	42.85
BVF gate	0.026	37.14	3.66	30.00
TR gate	0.031	25.83	18.58	40.00
1-bit Feynman gate comparator	0.026	32.50	10.36	3.00

the logic gates operated in constructing the circuit.

Applying a larger quantity of logic gates involves larger power dissipation by the circuits. The dispelled energy of the circuit is the total of the power dissipated by all the majority voters, inverters, and the range of QCA cells. The computation is achieved with the QCA power dissipation tool QCA Pro [43]. This paper, in spite of using the QCA Pro, mathematical analysis of Hamming distance-based assessment of power dissipation is applied to achieve the power dissipation of the proposed circuits. The assessment is achieved using the similar temperature (*i.e.*, $T = 2.0$ K) and the similar channelling energies (*i.e.*, $0.25E_k$, $0.75E_k$, *etc.*). It has been described [43] that, for a shift in the Hamming distance between inputs to the circuit, the energy dispelled will be differed too. In the case of the inverter, $1 \to 1$ or $0 \to 0$ input switching means Hamming distance '0', and the inverter has dispelled power of 0.8 meV at $\gamma = 0.25E_k$ and 2.7 meV at $\gamma = 0.5E_k$. For $1 \to 0$ or $0 \to 1$ input switching, Hamming distance '1' is considered for the inverter and the inverter has dispelled power of 28.4 meV at $\gamma = 0.25E_k$ and 28.6 meV at $\gamma = 0.5E_k$. A ceiling Hamming distance of '3' is measured for the

TABLE 5. Complexity of the proposed designs.

Proposed layout	Quantum cost	Area, μm^2	Latency	Quantum cost of proposed layout
XNOR gate	1	0.04	0.75	0.022
BVF gate	2	0.07	0.50	0.017
TR gate	4	0.12	1.00	0.120
1-bit Feynman gate comparator	1	0.08	0.50	0.020

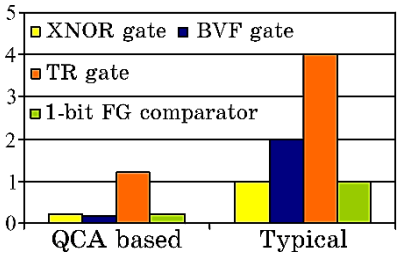

Fig. 9. Quantum cost of the proposed circuit and its QCA layout.

majority voter for $000 \rightarrow 111$ input switching that affects the ceiling dissipated energy of 41.0 meV by the majority voter at $\gamma = 0.25E_k$ and 41.2 meV at $\gamma = 0.5E_k$. Correspondingly, dissipation of power by the majority voter and inverter for several Hamming distances was testified in Refs. [44, 45]. The QCA design of the proposed XNOR consists of one inverter and three majority gates. Each of these majority voters has one stable input polarization.

Therefore, the Hamming distance for these majority voters is measured to be '2', correspondingly. For maximum energy dissipation, Hamming distance '1' is measured for each of the inverters. Applying the Hamming distances related to the input to logic gates and counting the QCA arrays perform in XNOR, the power dissipation of the proposed XNOR is analysed. The results are shown in Table 6. An equal method is applied for figuring the power dissipation by the BVF, TR and 1-bit Feynman gate comparator and the outcomes are denoted in Table 6. Table 6 illustrates that the power dissipated by the XNOR at $\gamma = 0.25E_k$ is of 79.3 meV, and at $\gamma = 1.0E_k$, it is of 94.6 meV. Similarly, for BVF gate, the dissipated power at $\gamma = 0.25E_k$ is of 260.4 meV, and at $\gamma = 1.0E_k$, it is of 295.6 meV; for TR gate, it is of 305.1 meV and 355.6 meV, correspondingly. The power dissipated by the proposed 1-bit Feynman gate comparator is of 206.7 meV when $\gamma = 0.25E_k$ and 235.6 meV when $\gamma = 1.0E_k$. Here, T is the temperature, γ stands for channelling energy, and E_k denotes the kink energy. These outcomes show that all the circuits dissipate very little heat energy. The results are also

TABLE 6. Energy dissipation by the proposed layouts.

Proposed design	$T = 2.0$ K (meV)			
	$0.25E_k$	$0.5E_k$	$0.75E_k$	$1.0E_k$
XNOR gate	79.3	82.8	88.3	94.6
BVF gate	260.4	270.8	275.2	295.6
TR gate	305.1	322.8	340.5	355.6
1-bit Feynman gate comparator	206.7	213.8	224.9	235.6

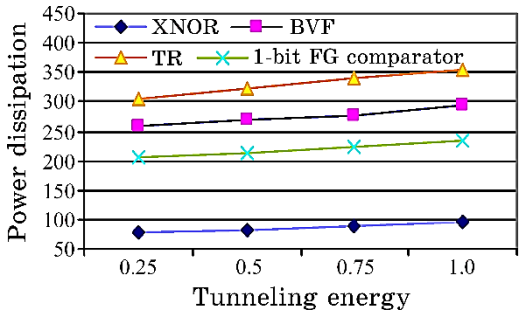

Fig. 10. Power dissipation by the proposed circuits ($T = 2.0$ K).

outlined in Fig. 10.

The average output polarization (AOP) of any cell of the QCA circuit is decreased by enhancing the temperature. The outcome of temperature on the AOP of the urged circuits is presented in Fig. 11. The AOP of the output cell P of the proposed XNOR is slowly lessened, up to a temperature of $T = 8$ K. TR gate work competently between 1 K and 4 K. Similarly, the BVF and 1-bit Feynman gate comparator circuit work proficiently between 1 K and 5 K.

To generate the AOP at separate temperatures, all the proposed designs are simulated by the QCADesigner tool [46] and the highest and lowest polarizations for each cell are observed.

For instance, at $T = 1$ K, the highest and lowest polarizations of output cell P of XNOR are of $9.54e^{-1}$ and $-9.52e^{-1}$, correspondingly. So, the AOP for cell P is of $[(9.54e^{-1})-(-9.52e^{-1})]/2 = 3.51$.

In the similar way, the AOP for separate cells of each proposed circuit at several temperatures are analysed as shown in Fig. 11.

6. CONCLUSION

QCA is an evolving nanotech where elements are micro sized and current clock speed on terahertz range. By uniting the excessive low power consumption of reversible computing and QCA, it is possible

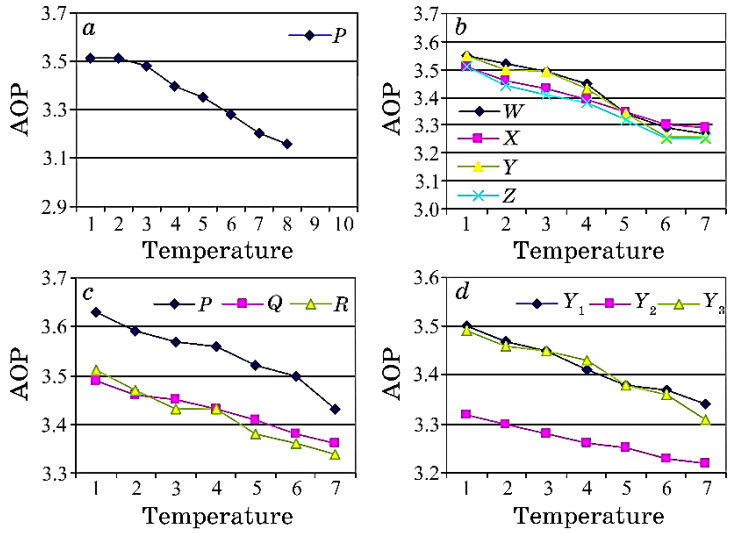

Fig. 11. Temperature effect on AOP of the proposed circuits: (*a*) XNOR, (*b*) BVF, (*c*) TR; (*d*) 1-bit Feynman gate comparator.

to design an extremely profitable logic device, which also apposite for reversible logic circuits.

This paper, a remarkable layout of XNOR, TR, BVF and 1-bit Feynman gate comparator is presented in QCA. The proposed XNOR, TR, BVF gate is 548, 592, 595 times reduced in area, correspondingly, than CMOS technology and flout multilayer wire crossing that would be extremely substantial for designing fault tolerant and compact low power expending nanomaterial.

For the first time, the power dissipation, quantum cost and constancy of the XNOR, TR, BVF and 1-bit Feynman gate comparator have been proposed in this paper.

The proposed QCA circuits exceed the existing ones in terms of cell complexity, area, and latency. The quantum cost-based assessment confirms that the proposed circuits have incredibly low quantum cost measure up to typical designs. The layouts have extremely low heat-energy dissipations, presenting that QCA nanomaterials are appropriate for applying reversible circuits.

The analysis of constancy of the proposed designs under thermal randomness exhibits the permanence of the circuits.

The assessment of simulation outcomes of the proposed circuit with theoretical significances verifies the functionality of the circuits.

The projected design can be used to achieve the nanoscopic scale reversible computing architecture in communication through low power consumption.

REFERENCES

1. J. A. Carballo, W. T. J. Chan, P. A. Gargini, A. B. Kahng, and S. Nath, *32nd International Conference on Computer Design—ICCD (19 October, 2014)*, p. 139; https://doi.org/10.1109/ICCD.2014.6974673
2. C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, *Nanotechnology*, **4**, Iss. 1: 49 (1993); https://doi.org/10.1088/0957-4484/4/1/004
3. N. Gallagher and G. Wise, *IEEE Trans. Acoust., Speech, Signal Process*, **29**, Iss. 6: 1136 (1981); https://doi.org/10.1109/TASSP.1981.1163708
4. E. Aptoula and S. Lefèvre, *Pattern Recognit.*, **40**, Iss. 11: 2914 (2007); https://doi.org/10.1016/j.patcog.2007.02.004
5. I. Grattan-Guinness, *Hist. Math.*, **31**, Iss. 2: 163 (2004); https://doi.org/10.1016/S0315-0860(03)00032-6
6. K. Michielsen and H. De Raedt, *Phys. Rep.*, **347**, Iss. 6: 461 (2001); https://doi.org/10.1016/S0370-1573(00)00106-X
7. V. Chatzis and I. Pitas, *IEEE Trans. Image Process.*, **19**, Iss. 7: 699 (2000); https://doi.org/10.1109/42.875192
8. K. Benkrid, A. Benkrid, and S. Belkacemi, *J. Syst. Archit.*, **53**, Iss. 4: 184 (2007); https://doi.org/10.1016/j.sysarc.2006.09.010
9. K. Konstantinidis, G. C. Sirakoulis, and I. Andreadis, *IEEE Trans. Syst. Man. Cybern. Part C*, **39**, Iss. 5: 520 (2009); https://doi.org/10.1109/TSMCC.2009.2020511
10. T. Cole and J. C. Lusth, *Prog. Quantum. Electron.*, **25**, Iss. 4: 165 (2001); https://doi.org/10.1016/S0079-6727(01)00007-6
11. M. Abdullah-Al-Shafi and A. N. Bahar, *5th Intl. Conf. on Informatics, Electronics & Vision (May 13, 2016, Dhaka, Bangladesh)*, p. 620; https://doi.org/10.1109/ICIEV.2016.7760076
12. P. D. Tougaw and C. S. Lent, *J. Appl. Phys.*, **75**, Iss. 3: 1818 (1994); https://doi.org/10.1063/1.356375
13. M. Abdullah-Al-Shafi and A. N. Bahar, *Cogent. Eng.*, **3**, Iss. 1: 1237864 (2016); https://doi.org/10.1080/23311916.2016.1237864
14. M. Abdullah-Al-Shafi, *Nanosistemi, Nanomateriali, Nanotehnologii*, **16**, Iss. 2: 289 (2018); http://dx.doi.org/10.15407/nnn.16.02.289
15. M. Abdullah-Al-Shafi, M. S. Islam, and A. N. Bahar, *Int. J. Comput. Appl.*, **128**, Iss. 2: 27 (2015); https://doi.org/10.5120/ijca2015906434
16. M. Abdullah-Al-Shafi, A. N. Bahar, F. Ahmad, and K. Ahmed, *Cogent. Eng.*, **4**, Iss. 1: 1349539 (2017); https://doi.org/10.1080/23311916.2017.1349539
17. M. Abdullah-Al-Shafi and A. N. Bahar, *Cogent Engineering*, **4**, Iss. 1: 1391060 (2017); https://doi.org/10.1080/23311916.2017.1391060
18. M. Abdullah-Al-Shafi and A. N. Bahar, *J. Nanoelectron. Optoelectron.*, **13**, Iss. 6: 856 (2018); https://doi.org/10.1166/jno.2018.2302
19. M. Abdullah-Al-Shafi and A. N. Bahar, *Int. Nano Lett.*, **9**, Iss. 3: 265 (2019); https://doi.org/10.1007/s40089-019-0279-1
20. M. Abdullah-Al-Shafi and A. N. Bahar, *J. Comput. Theor. Nanosci.*, **14**, Iss. 5: 2416 (2017); https://doi.org/10.1166/jctn.2017.6842
21. M. Abdullah-Al-Shafi and A. N. Bahar, *Sens. Lett.*, **17**, Iss. 7: 595 (2019); https://doi.org/10.1166/sl.2019.4117
22. M. Abdullah-Al-Shafi and A. N. Bahar, *J. Nanoelectron. Optoelectron.*, **14**, Iss. 9: 1275 (2019); https://doi.org/10.1166/jno.2019.2630
23. M. Abdullah-Al-Shafi and Z. Rahman, *Solid State Electron. Lett.*, **1**, Iss. 2: 73

(2019); https://doi.org/10.1016/j.ssel.2019.11.004
24. M. Abdullah-Al-Shafi, A. N. Bahar, M. A. Habib, M. M. R. Bhuiyan, F. Ahmad, P. Z. Ahmad, and K. Ahmed, *Ain Shams Eng. J.*, **9**, Iss. 4: 2641 (2018); https://doi.org/10.1016/j.asej.2017.05.010
25. M. T. Niemier, M. J. Kontz, and P. M. Kogge, *Proc. 37th Annual Design Automation Conference (June 5–9, 2000, Los Angeles, California, USA)*, p. 227; https://doi.org/10.1145/337292.337398
26. M. Crocker, X. S. Hu, M. Niemier, M. Yan, and G. Bernstein, *IEEE Trans. Nanotechnol.*, **7**, Iss: 3: 376 (2008); https://doi.org/10.1109/TNANO.2007.915022
27. M. Abdullah-Al-Shafi and A. N. Bahar, *Int. J. Inf. Technol. Comput. Sci.*, **10**, Iss. 10: 38 (2018); https://doi.org/10.5815/ijitcs.2018.10.05
28. Md. Abdullah-Al-Shafi, *Commun. Appl. Electron.*, **4**, Iss. 1: 20 (2016); http://dx.doi.org/10.5120/cae2016652004
29. J. L. Cardenas-Barrera, K. N. Plataniotis, and A. N. Venetsanopoulos, *Math. Probl. Eng.*, **8**, Iss. 1: 87 (2002); https://doi.org/10.1080/10241230211381
30. V. Mardiris and V. Chatzis, *J. Eng. Sci. Technol. Rev.*, **9**, Iss. 2: 25 (2016); https://doi.org/10.25103/jestr.092.05
31. R. Zhang, K. Walus, W. Wang, and G. A. Jullien, *IEEE Trans. Nanotechnol.*, **3**, Iss. 4: 443 (2004); https://doi.org/10.1109/TNANO.2004.834177
32. I. Amlani, A. O. Orlov, R. K. Kummamuru, G. H. Bernstein, C. S. Lent, and G. L. Snider, *Appl. Phys. Lett.*, **77**, Iss. 5: 738 (2000); https://doi.org/10.1063/1.127103
33. S. B. Tripathi, A. Narzary, R. Toppo, M. Goswami, and B. Sen, *J. Phys. Conf. Ser.*, **1039**, Iss. 1: 012028 (2018); https://doi.org/10.1088/1742-6596/1039/1/012028
34. M. Abdullah-Al-Shafi and R. Ziaur, *Solid State Electron. Lett.*, **1**, Iss. 2: 73 (2019); https://doi.org/10.1016/j.ssel.2019.11.004
35. S. Sheikhfaal, S. Angizi, S. Sarmadi, M. H. Moaiyeri, and S. Sayedsalehi, *Microelectron. J.*, **46**, Iss. 6: 462 (2015); https://doi.org/10.1016/j.mejo.2015.03.016
36. S. S. Ahmadpour, M. Mosleh, and S. Rasouli Heikalabad, *J. Supercomput.*, **76**, Iss. 12: 10155 (2020); https://doi.org/10.1007/s11227-020-03249-3
37. M. Abdullah-Al-Shafi, M. S. Islam, and A. N. Bahar, *Int. Nano Lett.*, **10**, Iss. 3: 177 (2020); https://doi.org/10.1007/s40089-020-00304-y
38. M. R. Hasan, R. Guest, and F. Deravi, *ACM Comput. Surv.*, **55**, Iss. 13: 1 (2023); https://doi.org/10.1145/3583135
39. M. S. Islam, M. Abdullah-Al-Shafi, and A. N. Bahar, *JOT-TT*, **3**, Iss. 2: 145 (2015); https://doi.org/10.15415/jotitt.2015.32010
40. M. S. Islam, M. Abdullah-Al-Shafi, and A. N. Bahar, *Int. J. Comput. Appl.*, **134**, Iss. 7: 1 (2016); https://doi.org/10.5120/ijca2016907711
41. A. N. Bahar, S. Waheed, and N. Hossain, *Springer Plus*, **4**, Iss. 1: 153 (2015); https://doi.org/10.1186/s40064-015-0928-4
42. R. Akter, N. Islam, and S. Waheed, *Int. J. Comput. Appl.*, **109**, Iss. 1: 41 (2015); https://doi.org/10.5120/19155-0591
43. M. Abdullah-Al-Shafi, A. N. Bahar, F. Ahmad, M. M. R. Bhuiyan, and K. Ahmed, *Data Brief.*, **11**, Iss. 1: 593 (2017); https://doi.org/10.1016/j.dib.2017.03.001
44. M. Abdullah-Al-Shafi and A. N. Bahar, *Act. Passiv. Electron. Compon.*, **2018**, Iss. 1: 1 (2018); https://doi.org/10.1155/2018/5062960
45. M. Abdullah-Al-Shafi and A. N. Bahar, *Int. J. Multimed. Ubiq. Eng.*, **11**, Iss. 8: 379 (2016); https://doi.org/10.14257/IJMUE.2016.11.8.38
46. M. Abdullah-Al-Shafi, R. H. Aneek, and A. N. Bahar, *Int. J. Grid. Distrib. Comput.*, **10**, Iss. 1: 43 (2017); https://doi.org/10.14257/ijgdc.2017.10.1.05